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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,513	08/27/2003	Kazuko Nishimura	60188-638	3989

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EXAMINER
VANNUCCI, JAMES

ART UNIT	PAPER NUMBER
2828	

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DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,513	NISHIMURA ET AL.	
	Examiner	Art Unit	
	Jim Vannucci	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6 and 10* is/are rejected.

7)☒ Claim(s) *2,3,7-9 and 11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8-27-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slawson et al.(5,488,621) in view of Tanioka(4,729,035).

Claim 1, figures 2(a), 2(b) and 5(a) of Slawson disclose a light-emitting circuit(12), a drive circuit(20) for driving the light-emitting circuit, a bias circuit(46) for adding a bias current to a pulse current outputted from the drive circuit, a light-receiving circuit(26) for receiving monitoring light outputted from the light-emitting circuit, an I/V conversion circuit(32) for subjecting an output from the light-receiving circuit to current-to-voltage conversion, a maximum-value detection circuit(36a) for detecting the maximum value of an output voltage of the I/V conversion circuit, an average-value detection circuit(40) for detecting the average value of the output voltage of the I/V conversion circuit, and a second comparator(180) for comparing the average value with a second reference value to feed back the comparison result to the bias circuit.

The first comparator disclosed in Slawson compares a difference signal to a reference value for feedback instead of comparing a maximum signal to a reference value. Slawson does disclose a maximum value detection circuit.

Figure 3 of Tanioka discloses a maximum value detection circuit with a first comparator(6) for comparing a maximum value(1) with a first reference value for improved compression processing of a signal(col. 5, lines 10-22).

Claim 4, Slawson discloses an initial-bias determination circuit for automatically setting an optimum initial bias value for the bias circuit(col. 4, lines 22-33).

Claim 5, Slawson discloses an adaptive drive circuit(56) for rapidly increasing or decreasing the pulse current and Tanioka discloses a maximum value circuit(1) that uses a difference between the maximum value detected by the maximum-value detection circuit and the first reference value.

Claim 6, Slawson discloses an adaptive bias circuit(46) for rapidly increasing or decreasing the bias current if a difference between the average value detected by the average-value detection circuit and the second reference value is large.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the comparator disclosed in Tanioka in the maximum value detection circuit disclosed in Slawson for improved signal processing as disclosed in Tanioka.

3. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Slawson in view of Tanioka as applied above, and further in view of Tachibana(5,710,750).

Claim 10, Slawson discloses a light-emitting circuit, a drive circuit for driving the light-emitting circuit, a bias circuit for adding a bias current to a pulse current outputted from the drive circuit, a light-receiving circuit for receiving monitoring light outputted from the light-emitting circuit, an I/V conversion circuit for subjecting an output from the light-

receiving circuit to current-to-voltage conversion, and a maximum-value detection circuit for detecting the maximum value of an output voltage of the I/V conversion circuit as referenced above.

Tanioka discloses a comparator for comparing the maximum value with a first reference value as referenced above.

Slawson and Tanioka do not disclose a duty detection circuit.

Figure 2 of Tachibana discloses a duty detection circuit(18) for detecting the duty ratio of an output voltage so as to feed back the detected duty ratio to obtain a desired duty ratio of the output voltage(col. 5, lines 38-46).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the duty detection circuit disclosed in Tachibana with the device disclosed in Slawson and Tanioka so that a desired duty ratio can be obtained for a voltage signal as disclosed in Tachibana.

Allowable Subject Matter

4. Claims 2-3, 7-9 and 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter. The following limitations are primarily responsible for distinguishing these claims over the prior art.

Regarding claim 2, the limitations concerning the second reference value being generated from the first reference value; regarding claim 3, the limitations concerning the second reference value being generated from the maximum value detected by the maximum-value detection circuit; regarding claims 7-8, the limitations concerning a threshold-current detection circuit which, if the maximum value of the output voltage of the I/V conversion circuit is larger than the first reference value, receives a signal from the first comparator, computes a threshold current based on the two maximum values and the two average values, and feeds back the computed threshold current to the bias circuit as recited in claim 7; regarding claim 9, the limitations concerning a first arithmetic unit for computing a time difference between the rising and falling edges of the output voltage, a second arithmetic circuit for computing a time difference between the rising and falling edges of the drive current and a third comparator for comparing outputs from the first and second arithmetic circuits with each other to feed back the comparison result to the bias circuit; regarding claim 11, the limitations concerning the duty detection circuit including a charge pump circuit for receiving the output voltage of the I/V conversion circuit; regarding claims 12-13, the limitations concerning the duty detection circuit including two average-value detection circuits for detecting the respective average values of the non-inverted and inverted output voltages of the I/V conversion circuit, and a comparator for comparing outputs from the average-value detection circuits with each other to feed back the comparison result to the bias circuit as recited in claim 12.

Correspondence

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Jim Vannucci whose phone number is (571) 272-1820.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center whose telephone number is (703) 308-0956.

Papers related to Technology Center 2800 applications only may be submitted to Technology Center 2800 by facsimile transmission. Any transmission not to be considered an official response must be clearly marked "DRAFT". The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center Fax Center number is (703) 872-9306.

James Vannucci